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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Docket Number (Optional)

BP2703

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on April 19, 2006

Signature /Bruce E. Garlick, 36,520/

Typed or printed name Bruce E. Garlick, 36,520

Application Number

10/731,803

Filed

Dec. 9, 2003

First Named Inventor

Li Fung Chang

Art Unit

2631

Examiner

Juan A. Torres

Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.

This request is being filed with a notice of appeal.

The review is requested for the reason(s) stated on the attached sheet(s).

Note: No more than five (5) pages may be provided.

I am the

- ☐ applicant/inventor.
☐ assignee of record of the entire interest.
See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed.
(Form PTO/SB/96)

☒ attorney or agent of record. 36,520
Registration number

☐ attorney or agent acting under 37 CFR 1.34.

Registration number if acting under 37 CFR 1.34

/Bruce E. Garlick, 36,520/

Signature
Bruce E. Garlick

Typed or printed name

512-264-88166

Telephone number

April 19, 2006

Date

NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below*.

☐ *Total of 1 forms are submitted.

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In the Application of:
Li Fung Chang

Serial No.: 10/731,803

For: EDGE INCREMENTAL
REDUNDANCY SUPPORT IN A
CELLULAR WIRELESS TERMINAL

§ Group Art Unit: 2631
§ Examiner: Juan A. Torres
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§ Filed: December 9, 2003
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REQUEST FOR REVIEW OF FINAL OFFICE ACTION

The Final Office Action mailed December 19, 2005 rejected claims 1 and 14 under 35 U.S.C. 102(b) as being anticipated by Pukkila (US 20010017904 A1). The Office Action rejected claims 1, 14, and 27 (among others) under 35 U.S.C. 102(e) as being anticipated by Parolari (US 20040081248 A1). Applicants disagree with these rejections and request review.

5 **Claims 1 is not anticipated under 35 U.S.C. 102(b) by Pukkila**

Independent claim 1 is directed to a “system for implementing Incremental Redundancy (IR) operations in a wireless receiver.” This system of claim 1 includes:

a baseband processor that is operable to receive analog signals corresponding to a data block and to sample the analog signal to produce samples;

10 an equalizer that is operable to receive the samples from the baseband processor, to equalize the samples, and to produce soft decision bits of the data block;

a system processor that is operable to receive the soft decision bits and to initiate IR operations; and

15 an IR processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits.

The Office Action equates block 203 of Pukkila (Ampl., A/D) with the baseband processor of claim 1. Block 203 of Pukkila is a combined amplifier and analog to digital converter. A

combined amplifier and analog to digital converter is simply not equivalent to a baseband processor. A baseband processor, in addition to performing amplification and analog-to-digital conversion operations, is capable of performing significant other baseband processing operations, as is described in the specification of the present application. Thus, the combined amplifier and analog
5 to digital converter of Pukkila block 203 does not equate to the baseband processor element of claim 1 and, for this reason, Pukkila does not anticipate claim 1.

The Office Action equates three elements of claim 1 with block 205' of Pukkila. Firstly, the Office Action equates the equalizer of claim 1 with block 205 (of block 205') of FIG. 2 of Pukkila. Secondly, the Office Action equates the system processor with block 205' of FIG. 2 (and operations
10 of FIG. 3) of Pukkila. Thirdly, the Office Action equates the IR processing module with block 205' of FIG. 2 (and operations of FIG. 3) of Pukkila. Equating block 205' with multiple claim elements is impermissible in making an anticipation rejection. Each teaching of a prior art reference can only be used to meet one claim element. Because block 205' is cited against multiple elements of claim 1, Pukkila does not anticipate claim 1.

15 Block 205' of FIG. 2 of Pukkila cannot be equated to either the system processor or the IR processing module of claim 1. As Pukkila describes at paragraph 25, last sentence, block 205' is a "turbo equalizer." Block 205' of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and reinterleaving operations. Block 205' is not "a system processor that is operable to receive the soft decision bits and to initiate IR operations" as required by claim 1. Block 205' is not "an IR
20 processing module operably coupled to the system processor that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits." Thus, Pukkila does not disclose either the system processor or the IR processing module of claim 1. For this reason, Pukkila does not anticipate claim 1.

Pukkila further fails to describe the interaction among the elements of claim 1. FIG. 3 of Pukkila does not describe how any of blocks of FIG. 2 receives soft decision bits and initiates IR operations as does the system processor of claim 1. Pukkila does not describe how any of the blocks of FIG. 2 receives soft decision bits and performs IR operations on the soft decision bits as
5 does the IR processing module of claim 1. For this reason as well, Pukkila does not anticipate claim 1.

Claims 14 is not anticipated under 35 U.S.C. 102(b) by Pukkila

Independent claim 14 is directed to a “system for implementing Incremental Redundancy (IR) operations in a wireless receiver.” This system includes:

- 10 (1) at least one processing device that is operable to receive an analog signal corresponding to a data block, to sample the analog signal to produce samples, to equalize the samples, to produce soft decision bits of the data block, and to initiate IR operations; and
- (2) an IR processing module operably coupled to the at least one processing device that is operable to receive the soft decision bits and to perform IR operations on the soft decision bits.

15 As was the case with the rejection of claim 1, the Office Action equates multiple elements of independent claim 14 with block 205’ of FIG. 2 (blocks 305-318 of FIG. 3 of Pukkila). Firstly, the Office action equates “at least one processing device” of claim 1 with block 205’ of FIG. 2 and FIG. 3 blocks 305-318 of Pukkila. Secondly, the Office action equates “an IR processing module” of claim 1 with block 205’ of FIG. 2 and FIG. 3 blocks 305-318 of Pukkila. Because block 205’ is
20 cited against multiple elements of claim 14, Pukkila does not anticipate claim 14.

Further, block 205’ of FIG. 2 of Pukkila cannot be equated to either the IR processing module of claim 14. As Pukkila describes at paragraph 25, last sentence, block 205’ is a “turbo equalizer.” Block 205’ of FIG. 2 of Pukkila performs equalization, deinterleaving, decoding, and

reinterleaving operations. Block 205' is not "an IR processing module operably coupled to the at least one processing device to receive the soft decision bits and to perform IR operations on the soft decision bits" as claim 14 requires. Thus, Pukkila does not disclose the IR processing module of claim 14. For this reason, Pukkila does not anticipate claim 14.

5 Pukkila further fails to disclose a processing device that initiates IR operations. While Pukkila discloses a method for performing IR operations, it fails to describe what structure of FIG. 2 could "initiate IR operations." Thus, Pukkila fails to "identically set forth" all elements of claim 14 and, for this reason, Pukkila fails to anticipate independent claim 14.

Claims 1, 14, and 27 are not anticipated under 35 U.S.C. 102(e) by Parolari

The Office Action cites FIG. 5 and related text of Parolari as anticipating claim 1. FIG. 5 of Paraolari illustrates a control processor, an equalizer, and an incremental redundancy buffer, among other elements. Claim 1 requires a baseband processor, an equalizer, a system processor, and an IR processing module. At best Paraolari discloses the system processor and equalizer of claim 1. Paraolari does not disclose an IR processing module and baseband processor that are distinct from the system processor and equalizer, as required by claim 1. Further, claim 1 requires that "the system processor is operable to receive the soft decision bits from the [the equalizer] and to initiate IR operations" and that the "IR processing module . . . is operable to receive the soft decision bits and to perform IR operations." Paraolari fails to disclose any separate elements that are operable to "initiate IR operations" and/or to perform IR operations.

Claim 14 requires the distinct elements of "at least one processing device" and "an IR processing module", the IR processing module operable to perform IR operations. Parolari does not disclose such distinct elements. Parolari does not disclose which of its elements performs IR processing operations, how they are initiated, or how they are accomplished.

Claim 27 is a method claim describing how IR processing is accomplished within a wireless receiver that includes an IR Processing module. As described with reference to claims 1 and 14, Parolari does not disclose a distinct IR processing module or its operations, as are required by claim 27.